Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

- 1. (original) A semiconductor die package comprising;
 - a semiconductor die;
 - a leadframe having a chemically-etched surface; and
 - a capsule enclosing said die and at least a portion said leadframe.
- 2. (original) The semiconductor package of Claim 1 wherein said leadframe consists essentially of copper alloy.
- 3. (original) A semiconductor die package comprising a semiconductor die, a leadframe having a roughened surface, and a capsule enclosing said die and at least a portion of said leadframe, wherein a surface of said leadframe is roughened by exposing said surface to a chemical etchant, thereby enhancing adhesion between said leadframe and said capsule.
- 4. (original) The semiconductor package of Claim 3 wherein said leadframe comprises copper alloy.
- 5. (original) The semiconductor package of Claim 4 wherein said chemical etchant comprises sulfuric acid.
- 6. (original) The semiconductor package of Claim 5 wherein said chemical etchant comprises hydrogen peroxide.
 - 7. (currently amended) <u>A The</u> semiconductor package of Claim 6 comprising:; a semiconductor die;
 - a leadframe having a chemically-etched surface; and
 - a capsule enclosing said die and at least a portion said leadframe;
 - said package further comprising an organo-metallic coating exide on the surface of the leadframe.

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8-20. (canceled)

- 21. (new) The semiconductor package of Claim 1 wherein the arithmetic mean deviation of a profile of said chemically-etched surface is in the range of 0.050 μm to 0.170 μm.
- 22. (new) The semiconductor package of Claim 21 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 μm to 0.700 μm.
- 23. (new) The semiconductor package of Claim 22 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm.
- 24. (new) The semiconductor package of Claim 21 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm.
- 25. (new) The semiconductor package of Claim 24 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm.
- 27. (new) The semiconductor package of Claim 22 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm.
- 27. (new) The semiconductor package of Claim 21 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm.
- 28. (new) The semiconductor package of Claim 1 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 μm to 0.700 μm.
- 29. (new) The semiconductor package of Claim 28 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm.
- 30. (new) The semiconductor package of Claim 29 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm.
- 31. (new) The semiconductor package of Claim 28 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μ m to 0.750 μ m.
- 32. (new) The semiconductor package of Claim 1 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μ m to 1.500 μ m.

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- 33. (new) The semiconductor package of Claim 32 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μ m to 0.750 μ m.
- 34. (new) The semiconductor package of Claim 1 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm.
- 35. (new) The semiconductor package of any one of Claims 21 to 34 further comprising an organo-metallic coating on the surface of the leadframe.

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